Amendments to the Specification:

Please replace the paragraph beginning on page 8, line 14, and ending on page 8, line 24, with the following amended paragraph:

FIGURE 3 is a block diagram illustrating examples of interface converter paddle 70, physical layer card 72, and line card section 64 of FIGURE 2. Interface converter paddle 70 is coupled to physical links 60, and may perform optical-to-electrical and electrical-to-optical conversions, if appropriate. Interface converter paddle 70 may comprise, for example, gigabit interface converters (GBIC) having any suitable port such as an InfiniBand, Ethernet, or Fibre Cannel port, that supports any suitable speed. In the illustrated example, physical layer card 72 performs physical layer conversions on data packets (such as data packet 90) or cells (such as cell 92), for example, clock recovery, framing, 10b/8b decoding, and deserialization. Interface converter paddle 70 and physical layer card 72 may accommodate any suitable number of links 60. In the illustrated example, physical links 60 are labeled link 0 though link 15.

Please replace the paragraph beginning on page 18, line 26, and ending on page 19, line 8, with the following amended paragraph:

Interface converter paddle 70 includes one or more transceivers 820, a programmable logic device 822, a memory 824, and discretes 826. A transceiver 820 receives optical data signal 812 through a port 813, transforms the optical data signals 812, which may comprise high-speed optical signals, into electrical data signals 814. According to one embodiment, transceiver 820 receives electrical data signals that do not require conversion. Transceivers [[810]] 820 may be selected to handle speeds appropriate to the communication protocol of interface converter paddle 70. For example, a transceiver 820 may be selected to handle one Gigabit Ethernet. A transceiver 820 may handle multiple speeds, which may be controlled by software commands. Programmable logic device 822 controls the operations of transceivers 820, and may comprise, for example, a complex programmable logic device (CPLD). Programmable logic device 822 communicates with a board surface controller 810 and executes commands received from board surface controller 810. Programmable logic device 822 may also determine the status of each port 813 of interface converter paddle 70.

Please replace the paragraph beginning on page 21, line 26, and ending on page 21, line 29, with the following amended paragraph:

A coupler 834 is coupled to transceivers [[810]] 820. Coupler 834 may comprise, for example, a small-form factor pluggable (SFP) transceiver right angle surface mount (SMT) receptacle or other suitable connector. Transceivers 820 and coupler 834 are coupled to substrate 852. A status indicator 854 indicates the status of interface converter paddle 70. Status indicator 854 may comprise, for example, light-emitting diodes (LEDs) and light pipes that channel the light from the light-emitting diodes to input-side panel 850. Board surface controller 810 determines that status and instructs programmable logic device 822 to indicate the appropriate status.

Please replace the paragraph beginning on page 22, line 27, and ending on page 23, line 7, with the following amended paragraph:

FIGURE 16 is a flowchart illustrating an example of a method for converting data signals. The method begins at step 880, where interface converter paddle 70 is coupled with physical layer card 72. Interface converter paddle 70 may be coupled by receiving interface converter paddle 70 in input-side panel 850 to couple high-speed coupler 828 to physical layer card 72. A communication protocol assisted with interface converter paddle 70 is identified at step 882. Programmable logic device 832 determines the communication protocol of interface converter paddle 70 and notifies board-surface controller 810 of the identified communication protocol. Board surface controller 810 in turn notifies serdes [[810]] 830 of the communication protocol. The clock frequency of serdes 830 is set according to the identified communication protocol at step 884. Board surface controller 810 determines the appropriate clock speed for the identified communication protocol and instructs programmable logic device 832 to set the clock frequency of serdes 830.

Please replace the paragraph beginning on page 23, line 8, and ending on page 23, line 13, with the following amended paragraph:

Data signals 812 are received by interface converter paddle 70 at step 886. Interface converter paddle 70 converts data signals 812 from optical data signals 812 to electrical data signals 814 at step [[888]] 887, if appropriate. Physical layer card 72 converts data signals 814 from serial data signals 814 to parallel data signals 816 at step [[890]] 888. Data signals 816 are transmitted to line card 54 at step [[892]] 889. After transmitting the data signals 816, the method terminates.

Please replace the paragraph beginning on page 23, line 14, and ending on page 23, line 24, with the following amended paragraph:

FIGURE 17 is a top view of ~~an example~~ a first exemplary embodiment of an interface converter paddle 890. Interface converter paddle 890 may support eight ports of, for example, one Gigabyte Fibre Channel, two Gigabyte Fibre Channel, one Gigabyte Ethernet, or 1X InfiniBand. Interface converter paddle 890 includes transceivers 820 with ports 813, programmable logic device 822, and coupler 828, coupled to substrate 852. Transceivers 820 may comprise eight small form factor pluggable transceivers, and may support differential data lines as fast as 2.4 Gbps. Transceivers 820 may include control pins for received loss of signal, transmit fault, transmit disable, rate select, and an interface to memory 824. The control pins may be coupled to programmable logic device 822 and may be controlled and monitored by board surface controller 810 via bus 821.

Please amend the paragraph beginning on page 23, line 31, and ending on page 24, line 10, with the following amended paragraph:

FIGURE 20 is a top view of ~~an example~~ a second exemplary embodiment of an interface converter paddle 892. Interface converter paddle 892 includes transceivers 820 with ports 813, programmable logic device 822, and coupler 828 coupled to substrate 852. Transceivers 820 may comprise two XGP Multisource Agreement (XGP MSA) compliant transceivers, and may support different data lines as fast as 3.1876 Gbps. Transceivers 820 may be arranged in a staggered manner on substrate 852. Transceiver 820 may include control pins that are accessed using a standard that is not supported by board surface controller 810, for example, a management data input/output (MDIO) standard, but is supported by programmable logic device 822. Alternatively, board surface controller 810 may be designed to support the standard. Interface converter 854 may support two ports of ten Gigabit Fibre Channel or ten Gigabit Ethernet.

Please replace the paragraph beginning on page 24, line 17, and ending on page 24, line 22, with the following amended paragraph:

FIGURE 23 is a top view of ~~an example~~ a third exemplary embodiment of an interface converter paddle 894. Interface converter paddle 894 includes transceivers 820 with ports 813, programmable logic device 822, and coupler 828 coupled to substrate 852. Interface converter paddle 854 may support two ports of 4X InfiniBand. Transceivers 820 may comprise two 4X parallel optics Multisource Agreement (MSA) compliant transceivers.

Please amend the paragraph beginning on page 25, line 7, and ending on page 25, line 12, with the following amended paragraph:

FIGURE 26 is a top view of ~~an example~~ a fourth exemplary embodiment of an interface converter paddle 900. Interface converter paddle 900 includes transceivers 820 with ports 813, programmable logic device 822, and serdes 830 coupled to substrate 852. Interface converter paddle 900 may support four 10G ports. Transceivers 820a-c may comprise XGP Multisource Agreement (XGP MSA) transceivers, and transceiver 820d may comprise a XENPAK Multisource Agreement (XENPAK MSA) transceiver.